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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/699,466	10/31/2000	Shunpei Yamazaki	0756-2222	8851

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EXAMINER
SARKAR, ASOK K

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 01/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/699,466	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *14 November 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 35-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 35-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *08/784,290* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *19* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims1 - 3 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 3, 35, 40, 43, 46 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa, US 5,728,259 in view of Masumo, US 5,306,651 and Takeuchi, US 5,661,056.

Regarding claims 1, 35, 40 and 43 Suzawa teaches a method of making a thin film transistor semiconductor device comprising the steps of:

- forming a semiconductor film on an insulating surface with reference to Fig. 2 in column 5, line 45;
- forming a semiconductor island having a tapered shape by patterning the semiconductor film having the tapered shape with an angle in the range of 20° to 50° between the side and the underlying surface as shown in Fig. 2A in column 6, lines 6 – 9;

- forming a gate insulating film of silicon oxide film on the surface of the semiconductor island by a second heating with reference to Fig. 2C in column 6, lines 20 – 22;
- forming a gate electrode 509 over the semiconductor island with the gate insulating film in between the island and the gate with reference to Fig. 5D in column 7, line 57;
- forming source and drain region in the semiconductor island with reference to Fig. 5E in column 8, lines 5 – 10;
- wherein irradiation of laser light is performed after forming the semiconductor film in column 5, lines 53 – 55.

Suzawa fails to teach forming a second gate insulating film of silicon oxide nitride over the first gate insulating film of silicon oxide.

Masumo teaches that during the formation of TFT, a single or a multilayer of silicon oxide and silicon oxide nitride can be made in column 4, lines 1 – 5.

Takeuchi teaches the advantages of multi-layer gate insulating film of oxide and oxide nitride in column 2, lines 21 – 28 since oxide nitride provides good withstand voltage characteristic.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's device by providing a second gate insulating film of silicon oxide nitride over the first gate insulating film of silicon oxide as taught by Masumo so that the withstand voltage characteristic of the gate is improved as taught by Takeuchi.

Regarding claim 2, Suzawa teaches the semiconductor film is a crystalline semiconductor film as described above in rejecting claim 1.

Regarding claim 3, Suzawa teaches patterning by an isotropic dry etching method in between column 5, line 61 and column 6, line 13.

Regarding claims 46 and 49, Suzawa teaches that the silicon film can be crystallized by heat annealing and followed by laser annealing.

Suzawa fails to teach laser irradiation is performed after forming the semiconductor island.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's method since improving the crystalline property can be better accomplished after forming the semiconductor island by crystallizing the film by heat only

4. Claims 36, 38, 41, 44, 47 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa, US 5,728,259 in view of Masumo, US 5,306,651; Takeuchi, US 5,661,056; Guldi, US 5,535,471 and Wolf, "Silicon Processing for the VLSI Era", Vol. 2, Chapter 4, last paragraph of page 274(1990).

Regarding claims 36, 38, 41 and 44, Suzawa teaches a method of making a thin film transistor semiconductor device comprising the steps of:

- forming a semiconductor film on an insulating surface with reference to Fig. 2 in column 5, line 45;
- forming a semiconductor island having a tapered shape by patterning the semiconductor film having the tapered shape with an angle in the range of 20° to

50° between the side and the underlying surface as shown in Fig. 2A in column 6, lines 6 – 9;

- forming a gate insulating film of silicon oxide film on the surface of the semiconductor island by a second heating with reference to Fig. 2C in column 6, lines 20 – 22;
- forming a gate electrode 509 over the semiconductor island with the gate insulating film in between the island and the gate with reference to Fig. 5D in column 7, line 57;
- wherein irradiation of laser light is performed after forming the semiconductor film in column 5, lines 53 – 55.

Suzawa fails to teach forming a second gate insulating film of silicon oxide nitride over the first gate insulating film of silicon oxide using mixed gases of TEOS and N_2O.

Masumo teaches that during the formation of TFT, a single or a multilayer of silicon oxide and silicon oxide nitride can be made in column 4, lines 1 – 5.

Takeuchi teaches the advantages of multi-layer gate insulating film of oxide and oxide nitride in column 2, lines 21 – 28 since oxide nitride provides good withstand voltage characteristic.

Guldi teaches silicon oxide nitride can be deposited by using TEOS in column 1, lines 35 – 38, TEOS is the Si source.

Wolf teaches that silicon oxide nitride can be deposited using N_2O as the source for nitrogen in the last paragraph of page 274.

Therefore, it would have been obvious to one with ordinary skill in the art at the

time of the invention to modify Suzawa's device by providing a second gate insulating film of silicon oxide nitride over the first gate insulating film of silicon oxide as taught by Masumo so that the withstand voltage characteristic of the gate is improved as taught by Takeuchi. For forming the gate insulating film of silicon oxide nitride mixed gases of TEOS and N_2O can be used as taught by Guldi and Wolf for the Si and the N sources.

Regarding claims 47 and 50, Suzawa teaches that the silicon film can be crystallized by heat annealing and followed by laser annealing.

Suzawa fails to teach laser irradiation is performed after forming the semiconductor island.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's method since improving the crystalline property can be better accomplished after forming the semiconductor island by crystallizing the film by heat only

5. Claims 37, 39, 42, 45, 48 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa, US 5,728,259 in view of Masumo, US 5,306,651; Takeuchi, US 5,661,056 and Yanagisawa, US 4,759,610.

Regarding claims 37, 39, 42 and 45, Suzawa teaches a method of making a thin film transistor semiconductor device comprising the steps of:

- forming a semiconductor film on an insulating surface with reference to Fig. 2 in column 5, line 45;
- forming a semiconductor island having a tapered shape by patterning the semiconductor film having the tapered shape with an angle in the range of 20° to

50° between the side and the underlying surface as shown in Fig. 2A in column 6, lines 6 – 9;

- forming a gate insulating film of silicon oxide film on the surface of the semiconductor island by a second heating with reference to Fig. 2C in column 6, lines 20 – 22;
- forming a gate electrode 509 over the semiconductor island with the gate insulating film in between the island and the gate with reference to Fig. 5D in column 7, line 57;
- forming an interlayer insulating film 611 of silicon nitride with reference to Fig. 6E in column 9, lines 6 – 8.
- wherein irradiation of laser light is performed after forming the semiconductor film in column 5, lines 53 – 55.

Suzawa teaches forming a silicon oxide layer 614 with reference to Fig. 6E in column 9, lines 13 – 14, but fails to teach forming a resin material layer over the interlayer insulating film 611.

Suzawa fails also to teach forming a second gate insulating film of silicon oxide nitride over the first gate insulating film of silicon oxide.

Masumo teaches that during the formation of TFT, a single or a multilayer of silicon oxide and silicon oxide nitride can be made in column 4, lines 1 – 5.

Takeuchi teaches the advantages of multi-layer gate insulating film of oxide and oxide nitride in column 2, lines 21 – 28 since oxide nitride provides good withstand voltage characteristic.

Yanagisawa teaches TFT containing display devices in which insulating films can also be formed of a organic material (resin) in column 5, line 16.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's device by providing a second gate insulating film of silicon oxide nitride over the first gate insulating film of silicon oxide as taught by Masumo so that the withstand voltage characteristic of the gate is improved as taught by Takeuchi. It would have been obvious also to one with ordinary skill in the art at the time of the invention to modify Suzawa's device by providing a second resin material insulating layer over the silicon nitride interlayer insulating material since making organic layer is more cost effective than making silicon oxide layer as taught by Yanagisawa.

Regarding claims 48 and 51, Suzawa teaches that the silicon film can be crystallized by heat annealing and followed by laser annealing.

Suzawa fails to teach laser irradiation is performed after forming the semiconductor island.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's method since improving the crystalline property can be better accomplished after forming the semiconductor island by crystallizing the film by heat only.

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11

F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1 – 3 and 35 - 51 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 - 38 of U.S. Patent No. 6,180,439 B1 in view of Suzawa, US 5,728,259; Masumo, US 5,306,651; Takeuchi, US 5,661,056; Guldi, US 5,535,471 and Wolf, "Silicon Processing for the VLSI Era", Vol. 2, Chapter 4, last paragraph of page 274(1990) and Yanagisawa, US 4,759,610.

Most limitations of these claims such as forming semiconductor film, crystallizing the film by first heating, patterning the film to an island/mesa shape, laser irradiating the semiconductor film, forming gate insulating film of silicon oxide are taught by the claims of Patent No. 6,180,439 B1.

Other aspects of the claims such as forming a second gate insulating film of silicon oxide nitride by reacting TEOS with N_2O, forming an interlayer insulating film of silicon nitride, covering it with a resin material, forming the gate, source and drains are covered by the additional references as were described earlier in rejecting these claims under 35 U.S.C. 103(a).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 703 308 2521. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 703 308 1233. The fax phone numbers for the organization where this application or proceeding is assigned are 703 308 7722 for regular communications and 703 308 7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 4918.

Asok K. Sarkar
January 16, 2003

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